WHAT IS CLAIMED IS:

1. A method for processing a semiconductor topography, comprising:

preferentially removing, in a region adjacent to an outer edge of the semiconductor topography, a portion of an upper layer of the topography; and

polishing the semiconductor topography such that its upper surface is substantially planar.

2. The method of claim 1, wherein the removed portion extends greater than approximately 3 mm inward from the outer edge of the semiconductor topography.

3. The method of claim 1, wherein the removed portion extends approximately 6 mm inward from the outer edge of the semiconductor topography.

4. The method of claim 1, wherein said peferentially removing comprises etching the portion of the upper layer.

5. The method of claim 1, wherein a thickness variation of a polished upper layer across the entirety of the semiconductor topography is less than approximately 500 angstroms.

6. The method of claim 5, wherein the thickness variation of a polished upper layer of the semiconductor topography is less than approximately 125 angstroms.

7. The method of claim 1, wherein said upper layer comprises a conductive material.

8. The method of claim 1, wherein said upper layer comprises a dielectric.

9. The method of claim 1, wherein said upper layer is formed upon and in contact with a polish stop layer prior to said removing, and wherein said polishing comprises exposing an upper surface of the polish stop layer.

10. The method of claim 1, wherein the upper layer is formed within a trench in the semiconductor topography, and wherein an upper surface of the upper layer in the trench is coplanar with an upper surface of a polish stop layer formed adjacent to the trench subsequent to said polishing.

11. The method of claim 1, wherein the upper layer is formed within a trench in the semiconductor topography, and wherein an upper surface of the upper layer in the trench is below an upper surface of a polish stop layer formed adjacent to the trench subsequent to said polishing.

12. The method of claim 4, further comprising forming a resist upon the upper layer and removing the resist in the region adjacent to the outer edge of the semiconductor topography to expose the portion of the upper layer prior to said etching.

13. The method of claim 12, wherein said removing the resist comprises applying an edge bead removal chemical to the resist in the region adjacent to the outer edge of the semiconductor topography.

14. The method of claim 12, wherein said removing the resist comprises exposing the resist in a region adjacent to the outer edge of the semiconductor topography and applying a developer to the resist.

15. The method of claim 12, further comprising stripping the resist prior to said polishing.

16. A semiconductor topography comprising an upper layer formed conformally upon a non-planar lower layer, wherein an average thickness of the upper layer in a region adjacent to an outer edge of the semiconductor topography is less than an average thickness of the upper layer in a region comprising a center of the topography.

17. The semiconductor topography of claim 16, wherein the region having a lower average thickness extends greater than approximately 3 mm laterally from the outer edge of the semiconductor topography.

18. The semiconductor topography of claim 16, wherein the average thickness of the upper layer in the region adjacent the outer edge is approximately 5% to approximately 30% less than the average thickness of the upper layer in the region comprising the center.

19. A semiconductor topography comprising a polished layer formed over a semiconductor wafer, wherein the polished layer comprises a plurality of structures, and wherein a thickness of a structure arranged within a region adjacent to an outer edge of the semiconductor topography differs by less than approximately 500 angstroms from a thickness of a corresponding structure arranged in a region comprising a center of the topography.

20. The semiconductor topography of claim 19, wherein the region adjacent the outer edge extends greater than approximately 3 mm laterally from the outer edge of the semiconductor topography.

21. The semiconductor topography of claim 19, wherein the structure within the region adjacent the outer edge is arranged approximately 4 mm from the outer edge.

22. The semiconductor topography of claim 19, wherein the structure comprises at least a portion of a semiconductor device.

23. The semiconductor topography of claim 19, wherein the plurality of structures are selected from the group consisting of gate structures, contact structures, local interconnect structures, conductive plugs, shallow trench isolation structures, dielectric layers, and conductive layers.